CLAIMS

1. A planar display panel comprising:

a first transparent substrate,

a pair of electrodes provided on said first transparent substrate, and

a second substrate having a recess formed in an area opposing to the pair of electrodes to define a discharge cell for a display cell.

2. A planar display panel according to Claim 1, wherein the pair of electrodes provided on said first transparent substrate is arrayed in plural number on said first transparent substrate in juxtaposed relation to form a group of electrodes.

3. A planar display panel according to Claim 1, wherein said recess is rectangular in shape and has a desired depth.

4. A planar display panel according to Claim 3, wherein said recess has a depth in the range of 300 - 600μm.

5. A planar display panel according to Claim 1, wherein a dielectric layer is formed on said first transparent substrate to cover the pair of electrodes.

6. A planar display panel according to Claim 1, wherein a fluorescent material layer is coated on a bottom surface of said recess formed in said second substrate.

7. A planar display panel according to Claim 6,

wherein a reflecting layer is interposed between the bottom surface of said recess formed in said second substrate and said fluorescent material layer.

8. A planar display panel according to Claim 1, wherein the pair of electrodes comprise a common electrode provided on said first transparent substrate for driving all of display cells together, which constitute a display screen, or for partly driving any plural number of the display cells at a time, and one of individual electrodes provided on the said transparent substrate for individually driving the display cells on the cell-by-cell basis which constitute the display screen.

9. A planar display panel according to Claim 8, wherein the depth of said recess formed in the second substrate is set to be three or more times a gap formed between said common electrode and said individual electrode for each display cell to produce discharge.

10. A planar display panel according to Claim 8, wherein evacuation grooves are formed to interconnect the display cells formed in said second substrate and an evacuation through hole is bored in said second substrate to be communicated with the evacuation grooves.

11. A planar display panel according to Claim 8, wherein lead pins are vertically provided on said common electrode and said individual electrodes in positions on

said first transparent substrate corresponding to between the display cells which constitute the display screen, and electrode leading-out through holes for leading out the lead pins to the back side of the display screen are bored in said second substrate in positions opposing to the lead pins.

12. A planar display panel according to Claim 11, wherein said lead pins are fused to bus electrodes of said individual electrodes and said common electrode by a paste or blazing material which is comprised primarily of the same metallic material as that of the bus electrodes of said individual electrodes and said common electrode.

13. A planar display panel according to Claim 11, wherein said lead pins each have a large-diameter base end portion which is fused to said electrode, and said electrode leading-out through holes each have a stepped shape comprising a large-diameter portion in which the base end portion of said lead pin is inserted, and a small-diameter portion through which a distal end portion of said lead pin is extended.

14. A planar display panel according to Claim 12, wherein a sealing guard is provided near a portion where said lead pins are fused, so that a sealing material is prevented from flowing into the display cells when an assembly of said first and second glass substrates is sealed off.

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15. A method for manufacturing a planar display panel, comprising the steps of:

patterning transparent electrodes of individual electrodes on a first transparent substrate,

forming bus electrodes of said individual electrodes and said common electrode on said first transparent substrate with said transparent electrodes formed thereon,

forming a dielectric layer to cover said individual electrodes and said common electrode on said first transparent substrate,

vertically fixing lead pins to said individual electrodes and said common electrode through electrode leading-out windows formed in said dielectric layer,

forming a protective film on said first transparent substrate having been subjected to said pin fixing step,

forming, in said second substrate, recesses for defining discharge spaces of display cells which constitute a display screen, electrode leading-out through holes for leading out said lead pins, which are vertically fixed to said common electrode and said individual electrodes, to the back side of the display screen, and an evacuation through hole,

forming fluorescent material layers on bottom surfaces of said recesses defining said display cells,

fitting said first and second substrates fabricated

through said steps to assemble a panel such that said lead pins on said first transparent substrate are extended to the outside via the through holes of said second substrate, and

sealing the assembled panel of said first and second substrates.

16. A controller for a planar display panel comprising a common electrode for driving all of display cells together, which constitute a display screen, or for partly driving any plural number of the display cells at a time, and individual electrodes for individually driving the display cells on the cell-by-cell basis, wherein said controller includes a driving circuit for changing luminance in accordance with the number of pulses applied to each of said individual electrodes within a unit time, thereby effecting gradation display.

17. A controller for a planar display panel according to Claim 16, wherein said driving circuit effects the gradation display based on control of application of a relatively wide sustaining pulse and a relatively narrow extinguishing pulse which are used as the pulses to be applied to each of said individual electrodes within the unit time.

18. A controller for a planar display panel according to Claim 16, wherein said planar display panel is constituted by display modules as constituent elements each

comprising a plurality of display units combined into a pattern of row-and-column matrix, said display modules arranged in the horizontal direction are cascaded, and a power supply is connected to said display modules in parallel, and

wherein a signal processing circuit for applying control signals to driving circuits of each of said display modules comprises:

an address information storage unit for storing specific address information,

an input signal control unit for allowing input data to pass through said control unit and taking data, which the display module including said control unit is to represent by itself, out of a position indicated by the specific address and a display effective signal in the data,

a through data output buffer for outputting the data, which has passed through said input signal control unit, to the adjacent display module cascaded downstream,

a memory into which the data taken out of said input signal control unit is written in response to a write control signal, and from which the data is read in response to a read control signal,

a display pulse generator for generating common electrode and individual electrode driving pulses based on the data taken out of said input signal control unit,

a counter for counting the common electrode driving pulse output from said display pulse generator,

a look-up table for converting the number of pulses counted by said counter into a numerical value of gradation data,

a display data generator for outputting individual electrode control data based on comparison between the gradation data from said look-up table and the individual electrode driving display data read from said memory, and

an output buffer for outputting outputs of said display pulse generator and said display data generator to individual electrode driving circuits and common electrode driving circuits.

19. A method for driving a planar display panel in which a pair of a common electrode driven in common and an individual electrodes driven individually are provided side by side for each of a plurality of cells, and a voltage pulse is applied to said common electrode to produce luminescence due to discharge on a dielectric layer formed over said common electrode and said individual electrode, said method comprising the steps of:

applying a voltage pulse to said individual electrode to reverse the polarity of wall charges accumulated on said dielectric layer, and

then applying a voltage pulse to said common electrode

so that an electric field of the wall charges caused upon the reversal of the polarity is additionally applied.

20. A method for driving a planar display panel according to Claim 19, wherein assuming that one sequence is defined by a certain number of voltage pulses applied to said common electrode, said voltage pulse is applied to said individual electrode in units of one or plural sequences.

21. A method for driving a planar display panel according to Claim 19, wherein the voltage pulse applied to said common electrode functions to start discharge at rising of the voltage pulse as a result of addition of the electric field of said wall charges caused upon the reversal of the polarity, and to produce erase discharge at falling of the voltage pulse with wall charges caused by the started discharge.

22. A method for driving a planar display panel according to Claim 21, wherein the voltage pulse applied to said common electrode is a composite voltage pulse comprising a first voltage pulse not higher than the discharge starting voltage and a second voltage pulse superposed within a period of said first voltage pulse, said composite voltage pulse having a voltage value not less than the discharge starting voltage.

23. A method for driving a planar display panel according to Claim 22, wherein erase discharge is produced

due to said wall charges at falling of said first voltage pulse.

24. A method for driving a planar display panel according to Claim 23, further comprising the step of applying the voltage pulse to said individual electrode to stop the discharge after erase discharge has been produced by said composite voltage pulse applied to said common electrode.

25. A method for driving a planar display panel according to Claim 19, wherein when the voltage pulse is applied to said common electrode to produce discharge, a voltage in a discharge sustaining region is applied to the individual electrode of the display cell in which the discharge is to be sustained, and a voltage in a discharge suppression region is applied to the individual electrode of the display cell in which the discharge is to be stopped.

26. A method for driving a planar display panel according to Claim 20, wherein assuming that one sequence is defined by a certain number of voltage pulses applied to said common electrode, gradation display is made by applying a voltage in a discharge sustaining region enough to sustain the discharge to the individual electrode corresponding to the number of voltage pulses in one part of one sequence, thereby providing a display sustaining period, and by applying a voltage in a discharge suppression region to stop

the discharge to the individual electrode corresponding to the number of voltage pulses in the other part of one sequence, thereby providing a display suppression period.

27. A method for driving a planar display panel according to Claim 26, wherein the front half of one sequence provides said display sustaining period and the second half of one sequence provides said display suppression period.

28. A method for driving a planar display panel according to Claim 26, wherein the certain number of voltage pulses applied to said common electrode within one sequence is selected to be not less than the certain number of gradation steps, and a plural number of voltage pulses are assigned to one gradation step.

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